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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,083	07/24/2003	Amit Ramchandran	021202-003730US	3515
37490	7590	12/13/2005	EXAMINER	
CARPENTER & KULAS, LLP 1900 EMBARCADERO ROAD SUITE 109 PALO ALTO, CA 94303			COLEMAN, ERIC	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/628,083

Applicant(s)

RAMCHANDRAN, AMIT

Examiner

Eric Coleman

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 13-20 is/are rejected.
- 7) ☒ Claim(s) 11 and 12 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fraser (patent No. 6,907,598) in view of Santhanam (patent No. 5,704,053).

3. Fraser taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Identifying frequently executed instruction in the set of instructions for an information processing device (e.g., see fig. 5); and

b) Replacing at least one instance of the frequently executed instruction with a compressed instruction referencing and index value (e.g., see fig. 5 and col. 3, lines 9-32 and col. 12-30).

4. Fraser further taught (claim 1) that the repeated instruction sequences were replaced with a compressed instruction (e.g., see col. 3, lines 9-32), but did not expressly detail inserting an explicit caching instruction in the set of instructions before the identified instruction, wherein the explicit caching instruction associates the identified instruction with at least one index value. Santhanam however taught inserting an explicit prefetching instruction in a loop of instructions to initiate prefetching of data needed in further loops not likely to be available in the cache (e.g., see col. 5, line 44-

col. 6, line 18). Here the Santhanam prefetching instruction was placed in the instruction sequence before the further loop instructions would have appeared in the program.

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Fraser and Santhanam. One of ordinary skill would have been motivated to incorporate the Santhanam teachings of inserting an explicit caching or prefetch instruction at least to ensure that compressed code would have been available in the cache when the compressed instruction was encountered in the program, which would have required retrieval of the uncompressed code and would have reduced the time taken to retrieve the code when the code was not in the cache. As to placing the explicit caching instruction before the compressed instruction, one of ordinary skill would have been motivated to place the explicit caching instruction there so that there would be time for the data to be prefetched and therefore be available when the compressed instruction was available just as the explicit prefetch instruction was placed before the further loop instructions in the program in the Santhanam teachings.

6. As per claim 2, Fraser taught the step of identifying includes identifying a subset from the set of instructions comprising a plurality of instructions (e.g., see col. 3, lines 9-32).

7. As per claim 3, Fraser taught the subset comprises a plurality of consecutive instructions from the set of instructions (e.g., see col. 3, lines 9-32).

8. As per claim 4, Santhanam taught the explicit caching instruction directs an information processing device to store the subset of instructions stored in the storage

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unit in association with at least one index value (e.g., see col. 5, line 44-col. 6, line 67).

9. As per claim 5, Santhanam taught the instruction storage element associated with the index value, such that the subset of instructions stored in the storage element can be retrieved with reference to the index value (e.g., see col. 17, lines 6-66).

10. As per claim 6, Santhanam taught the instruction storage unit has a plurality of storage elements, each storage element associated with an index value and explicit caching instruction directed information processing device to store each instruction of the subset of instruction in one of the plurality of storage elements, such that each one of the instructions can be retrieved with reference to the index value associated with the storage element (e.g., see col. 17, lines 6-66 and col. 7, lines 9-35).

11. As per claim 7, Santanam taught prefetching loops of instructions which would have been recognized by one of ordinary skill to applicable to outer loop subset and the subset of instructions part of an inner loop (e.g., see col. 5, line 44-col. 6, line 10). One of ordinary skill would have been motivated to utilize the prefetching of the inner loops to take advantage of the reduced time for access to loop instructions when processing a nested loop of instructions.

12. As per claim 8, Santanam taught the explicit caching instruction directs a node in an adaptive computing machine to store the identified instruction in an instruction storage unit in association with the index value (e.g., see col. 5, line 44-col. 6, line 67).

13. As per claim 9, Santhanam taught the instruction storage unit has a storage element associated with the index value, such that the subset of instructions stored in

the storage element can be retrieved with reference to the index value (e.g., see col. 17, lines 6-66).

14. As per claim 10, Fraser taught the compressed instruction directs an information processing device to execute the identified instruction associated with the index value (e.g., see col. 10, lines 12-30).

15. Claims 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Santhanam (patent No. 5,704,053) in view of Fraser (patent No. 6,907,598).

16. As per claim 13, Santhanam taught retrieving a primary instruction within a set of instructions from memory (e.g., see col. 6, lines 32-67); storing the at least one instruction subsequent to the primary instruction with the primary instruction is an explicit caching instruction (e.g., see col. 10, lines 2-18).

17. Santhanam did not specifically detail retrieving and executing at least one previously stored instruction when the primary instruction is a compressed instruction. Fraser however taught this limitation (e.g., see fig. 7 and col. 17, line 16-col. 18, line 51).

18. It would have been obvious to one of ordinary skill in the DP art in the DP art to combine the teachings of Santhanam and Fraser. One of ordinary skill would have been motivated to incorporate the Fraser teachings of storing the instructions identified to be frequently used and to be retrieved later in compressed form. This would have provided the combined system with reduced sized of an instruction stream (e.g., see col. 1, lines 15-40 of Fraser) which especially useful when small systems with limited amount of memory are implemented using the teachings of Santhanam and Fraser.

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19. As per claims 14, 19 Santhanam taught the explicit caching instruction directs an information processing device to store the subset of instructions from the set of instruction (e.g., see col. 5, line 44-col. 6, line 67). Considering the Fraser teaching of compressing the instruction and retrieving the instruction for execution, the processing of compressed instruction would have retrieved and executed with an association with the index especially when the compressed instruction comprised instructions of a loop such was taught by Santhanam.

20. As per claim 15,16,17,18 Santhanam taught the explicit caching instruction stores a subset comprising a plurality of consecutive instructions from the set of instructions in association with an index value in plural storage elements (e.g., see col. 5, line 44-col. 6, line 67) each storage element associated with an index value, such that each one of the instructions can be retrieved with reference to the index value associated with the storage element (e.g. see col. 17, lines 16-66).

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

22. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by De Oliveira Kastrup Pereira et al (patent No. 6,721,884) (here after referred to as De Oliveira).

De Oliveira taught the invention as claimed including a data processing ("DP") system comprising a configuration storage unit (e.g., see col. 6, lines 1-67 and col. 1, line 66-col. 2, line 7); sequencer (23)(e.g., see col. 5, line 18-col. 6, line 19) and functional unit (16)(e.g., see col. 4, lines 28-38). The claimed characteristics or functions performed in the claims are claimed in an "adapted to" characteristics or functions. These features are not positively claimed and therefore are not given any weight. The DeOliveira system comprises a processing system that comprises each element in the claimed invention and therefore is inherently capable of performing the claimed operations.

Allowable Subject Matter

23. Claims 11-12, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Budrovic (patent No. 6,865,664) disclosed a system for compressing a computer program based on a compression criterion (e.g., see abstract).


Worley (patent No. 4,713,755) disclosed a cache memory consistency control with explicit software instructions (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC



ERIC COLEMAN
PRIMARY EXAMINER